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# ANALYSIS AND DESIGN OF INDUCTORS FOR PROTECTING POWER TRANSISTORS AGAINST CURRENT SURGES IN INVERTER BRIDGE CIRCUITS

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## ABSTRACT

An analysis of transistor inverter and converter bridge circuits shows that surge currents exist during the switching time interval. And these currents result from transistor unequal turnon and turnoff switching characteristics. The surge currents are limited only by the resistance of the power source and the saturated resistance of the transistors. They can reach peak values which exceed the transistor's maximum-current rating by an order of magnitude. Inductors avoid transistor failure by limiting the current surges to safe levels. They also substantially reduce the circuit power loss due to the surge currents. A technique for the design of inductors with the proper inductance is presented.

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## SUMMARY

Transistor inverter bridge circuits are analyzed to determine the magnitude of current surges which cause catastrophic transistor failures. The particular currents of concern here are termed shoot-through currents. These currents occur during the time interval the transistors are being switched. They result from the unequal turnon and turnoff switching characteristics of the transistors. During the switching interval, both transistors in a given leg of a bridge circuit are conducting at the same time. And they produce a short circuit across the power source. The shoot-through current surge which flows in the bridge leg is limited only by the internal resistance of the power source and the saturated resistance of the transistors. In bridge circuits with paralleled transistors, the shoot-through currents increase in some transistors as other transistors turn off, and the slowest-switching transistor carries the total shoot-through current surge of the entire group. The shoot-through currents can reach peak values which exceed the safe maximum-current rating of the transistors.

The protective inductor is connected in series with the transistors it protects and limits the buildup of the shoot-through current during the switching interval. The buildup is limited to a peak level within the safe maximum-current rating of the transistor. The inductor thereby avoids those current levels and operating conditions that lead to catastrophic failure. A design method described leads to inductors with the proper inductance for safe and reliable circuit operation.

The analysis and design method presented are based on the success of the protective inductors in eliminating transistor failures due to shoot-through currents in an experimental high-frequency pulse-width-modulated inverter. They identify the problems associated with shoot-through currents and provide a practical means of limiting these currents to safe values.

# INTRODUCTION

Power transistors that operate in the switching mode in static power conditioning inverters and converters generally exhibit unequal switching characteristics; the turnon is considerably faster than turnoff. This difference is due mainly to the charge stored within the base region of the transistor during conduction. This charge must be removed before the transistor ceases conduction. The difference in switching times varies for transistors according to type and even among transistors of a given type according to production and fabrication variables. The time difference can vary from a few tenths of a microsecond for high-speed transistors to several microseconds for medium- and slower-speed transistors.

The unequal switching characteristics of transistors is troublesome in specific circuit applications and results in excessively high-current spikes through the transistors. When the transistors in a given leg of a bridge circuit are being switched, a short circuit across the power source is created by the rapid turnon of one transistor and the delayed turnoff of the other. The resulting current spike through the transistors is limited only by the impedance of the source and the saturated resistance of the transistors. In applications in which transistors are paralleled, the surge current increases through the slower transistors as the faster transistors switch off, and the slowest transistor in the group carries the total current spike when the others are off. The current spikes for each of these configurations reach exceptionally high levels and greatly exceed the safe maximum-current ratings of the transistors. The current spikes can lead to catastrophic transistor failure by excessive power dissipation at the collector-to-emitter junction, by secondary breakdown in the active region of the operating characteristics (ref. 1), or by formation of a localized hot-spot. The hot-spot distorts the characteristic and leads to failure by secondary breakdown (ref. 2). Catastrophic transistor failures were experienced with an experimental pulse-width-modulated inverter (ref. 3, p. 15). In the output power stages, the inverter utilized a bridge circuit which operated at a carrier frequency of 10 kilohertz. The failures were traceable to short-circuit current surges that resulted from the unequal switching characteristics of the transistors. The current surges are called "shoot-through currents." Various techniques have been developed to circumvent the shoot-through current problems and thereby to improve the reliability of inverter bridge circuits. One technique is to reduce the storage time of the transistors by means of a negative current through the base circuit of the transistor during the switching interval. The negative current quickly removes the stored charge in the base region and reduces the turnoff time (ref. 4, pp. 256-257). Another technique is to delay the turnon of the transistors for a period of time equal to or greater than the turnoff time (ref. 3, pp. 16-41). The turnon delay is produced by means of logic circuits or by the use of a saturable reactor. This technique effectively prevents shoot-through currents, but the

delay time results in a notch, or dwell, in the square-wave output voltage. In inverters for which the square wave is filtered to produce a sinusoidal output voltage, this notching is objectionable because the increased waveform distortion requires a larger filter. The technique used in the experimental inverter of reference 3 was to connect a reactor[1] in series with the transistors in each leg of the bridge. The reactor limits the transistor current during the switching interval to a level below the transistor's safe maximum-current rating. The reactors were very effective in eliminating transistor failures due to shoot-through currents. The analysis of their operation and method of design form the basis for this report.

This analysis identifies the switching interval and the shoot-through current spikes, and determines the required inductance of the reactor for safe operation. The design method presents a basis for selecting the magnetic core material and the means for designing the reactors with the proper inductance. The exact equations for shoot-through currents are derived in appendix A. The application of the reactor analysis and design method to a practical single-phase bridge inverter circuit is detailed in appendix B.

## SYMBOLS

| | |
|---|---|
| $A$ | area |
| $AT$ | ampere turns |
| $\Delta AT$ | change in ampere turns |
| $A_c$ | cross-sectional area of core, $cm^2$ |
| $A_g$ | area of air gap, $cm^2$ |
| $B$ | flux density, G or lines/$cm^2$ |
| $\Delta B$ | change in flux density |
| $D_D$ | diode rectifier for discharge current |
| $D_R$ | diode rectifier for reactive current |
| $E$ | voltage |
| $E_L$ | average reactor voltage |
| $e_L$ | instantaneous reactor voltage |
| $f$ | frequency, Hz |

[1]Reactor as used in this report is a device used in electrical and electronic circuits. It consists of a magnetic core and a winding of N-turns of insulated wire conductors. This is in contrast to a nuclear reactor.

| | |
|---|---|
| $H$ | magnetizing force, Oe |
| $\Delta H$ | change in magnetizing force |
| $I$ | current |
| $\Delta I$ | change in current |
| $I_B$ | transistor base current |
| $I_c$ | collector output current |
| $I_L$ | load current |
| $I_p$ | shoot-through current |
| $I_{p,\,max}$ | maximum shoot-through current |
| $I_{p,\,t}$ | total shoot-through current through leg of bridge with bank of paralleled transistors |
| $I_{p,\,1}, I_{p,\,2}, \ldots, I_{p,\,n}$ | shoot-through current through given leg of bridge |
| $i_d$ | reactor discharge current |
| $i_1, i_2, \ldots, i_m$ | instantaneous current through reactor |
| $L$ | inductance of reactor, H |
| $L_1, L_2, \ldots, L_n$ | reactor |
| $l$ | length, cm |
| $l_c$ | length of magnetic core |
| $l_g$ | length of air gap |
| $m$ | number of transistors still conducting in paralleled bank that is turning off |
| $N$ | number of turns in coil winding on core |
| $NI$ | magnetomotive force (mmf), ampere turns |
| $N\,\Delta I$ | change in magnetomotive force |
| $n$ | number of paralleled transistors |
| $P_{avg}$ | average power, W |
| $P_c$ | transistor power rating |
| $Q$ | transistor |
| $R$ | electrical resistance |

| | |
|---|---|
| $\mathscr{R}$ | reluctance of magnetic circuit, $l/\mu A$ |
| $R_b$ | internal resistance of battery |
| $R_{cs}$ | saturated transistor resistance |
| $R_D$ | discharge resistor |
| $R_L$ | load resistor |
| T | transformer |
| t | time, sec |
| $\Delta t$ | switching interval - period of time when all transistors in bridge circuit are conducting simultaneously |
| $t_D$ | time constant of discharge circuit, $L/R_D$ |
| $t_d$ | transistor turnon delay time |
| $t_f$ | transistor turnoff fall time |
| $t_o$ | time when transistor drive voltages initiate switching interval |
| $t_{off}$ | transistor total turnoff time |
| $t_{on}$ | transistor total turnon time |
| $t_p$ | period of operating frequency, s |
| $t_r$ | transistor turnon rise time |
| $t_s$ | transistor turnoff storage time |
| V | voltage across leg of bridge |
| $V_B$ | battery voltage |
| $V_{BE}$ | drive voltage applied to base-emitter junction |
| $V_{CB}$ | collector to base voltage |
| $V_{CE}$ | collector to emitter voltage |
| $V_{EB}$ | emitter to base voltage |
| $V_L$ | output load voltage |
| $\mu$ | permeability of magnetic material, $\Delta B/\Delta H$ |
| $\mu_c$ | permeability of magnetic core |
| $\mu_g$ | permeability of air gap, 1.0 |
| $\tau_1, \tau_2$ | time constants, sec |
| $\varphi$ | magnetic flux, lines or Mx |

$\Delta\varphi$ change in flux

$\varphi_c$ flux due to maximum shoot-through current

$\varphi_L$ flux due to load current

$\varphi_r$ remanent flux at zero current

$\varphi_{sat}$ saturation flux

# CIRCUIT OPERATION

## Bridge Circuit

A typical single-phase bridge inverter circuit with power-switching transistors is shown in figure 1. This circuit converts the dc voltage of the power source to a square-wave ac output voltage at the load. Transistors $Q_1$ and $Q_2$ comprise one leg of the bridge and $Q_3$ and $Q_4$ the other leg. The transistors operate in the switching mode and are controlled by the square-wave drive voltages applied to the base of each transistor. The drive voltages are obtained from separate windings on the common driver transformer $T_1$. These windings are connected to switch the diagonal transistor pairs ($Q_1$ - $Q_4$ and $Q_2$ - $Q_3$) on and off together and so that only one transistor in each leg of the bridge is turned on at a given time. Diode rectifiers $D_R$ are reactive diodes and

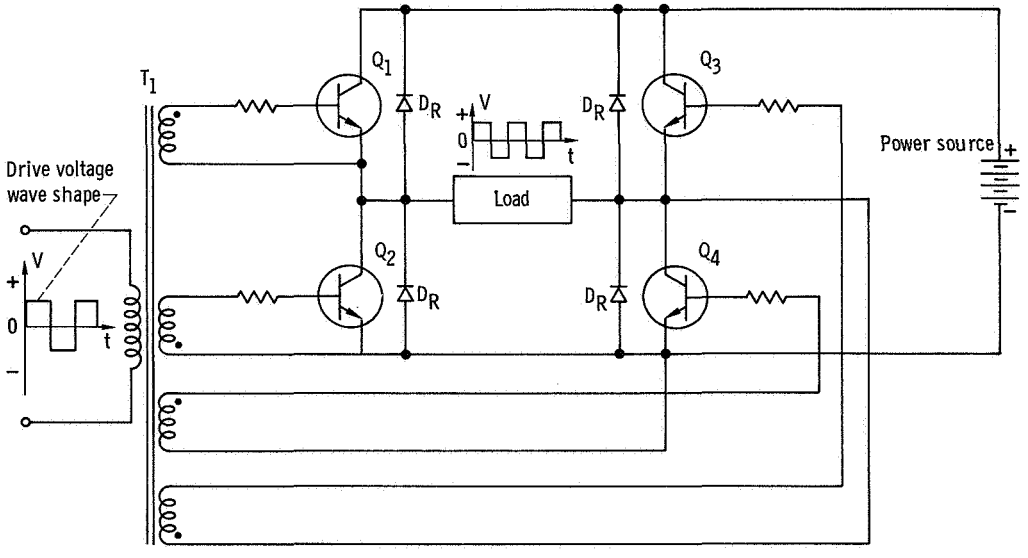



Figure 1. - Single-phase bridge.

provide an electrical path through the battery for the lagging reactive currents of inductive loads.

Each of the power transistors can be paralleled with additional transistors to increase the power-handling capability of the circuit. The switching action is the same, but in this case each transformer winding controls the switching of the entire parallel bank as a unit. The circuit operation is the same as for single transistors but is at a higher power output level.

## Transistor Switching Characteristics

Power transistors such as may be used in the circuit of figure 1 do not switch instantaneously as ideal switches, but rather they require discrete intervals of time to complete their switching from the "on" state to the "off" state and vice versa. These time delays are identified in figure 2, which shows the typical switching characteristics of a single power transistor (ref. 4, p. 248). The transistor is connected in a series circuit with a battery and resistive load and is switched to saturation and cutoff by a square-wave drive voltage. The upper trace of figure 2 is the drive voltage $V_{BE}$ applied to the base-emitter junction, and the lower trace is the response of the collector output current $I_c$.

The response trace illustrates four time intervals that the collector current undergoes in switching on and off. The turnon time consists of the delay and rise time intervals $T_d$ and $T_r$. The turnoff time consists of the storage and fall time intervals $T_s$ and $T_f$.

The collector current response trace also illustrates that the turnon and turnoff times are not equal; the turnoff time is considerably longer than the turnon time. The ratio of turnoff to turnon times for practical power transistors is typically of the order of 7 to 1, and the longer turnoff time is due mainly to the storage time. The storage time can be

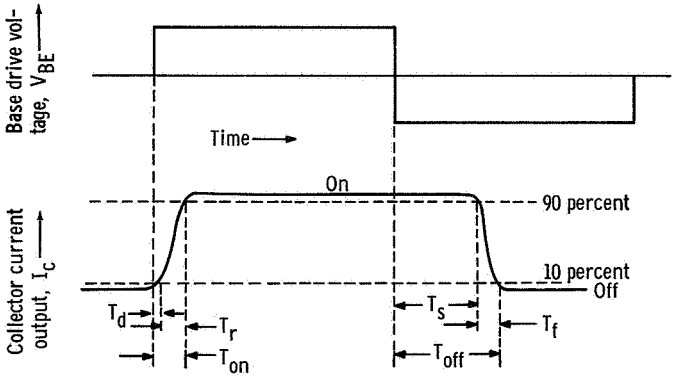



Figure 2. - Transistor switching characteristics.

reduced to a limited extent by the application of some techniques that may effect the overall performance of a specific circuit application. These include (1) operating the transistor unsaturated but just on the edge of saturation, and (2) by increasing the magnitude of the negative base current to sweep out the base charge at a faster rate (ref. 4, p. 248). Unsaturated operation reduces circuit efficiency by increasing transistor conduction losses. Increased base current requires additional circuitry to provide either a nonsymmetrical base drive waveform or a special base sweep-out current. Because of efficiency and reliability considerations then, the effects of the transistor's unequal switching characteristic must be evaluated with respect to the specific circuit application and the performance desired.

## Switching Interval

The unequal switching characteristic of power transistors is particularly troublesome in bridge circuits because it creates a condition where both transistors in a given leg are on at the same time and thereby provides a short-circuit path across the power source. This condition is illustrated by the sketches in figure 3 where the response of both transistors during switching are superimposed. The bridge leg consisting of transistors $Q_1$ and $Q_2$ in figure 1 is used for this discussion. The upper and lower traces of figure 3 represent the base drive voltages applied to transistors $Q_1$ and $Q_2$, respectively.

The transistor states just prior to switching are that $Q_1$ is on and conducting cur-

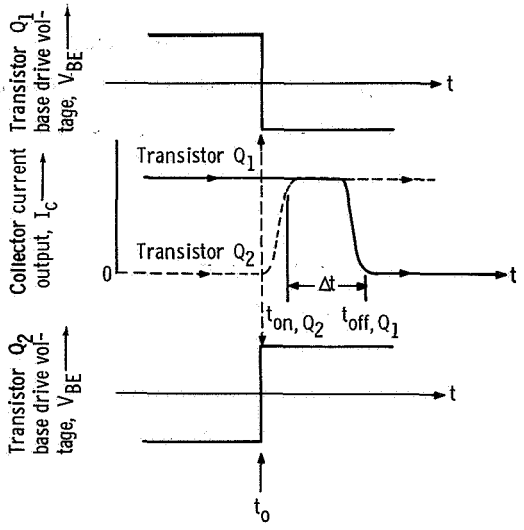



Figure 3. - Superposition of switching characteristics for both transistors in leg of bridge circuit during switching interval.

rent and $Q_2$ is off and nonducting. At time $t_o$, the base of $Q_1$ is reverse biased to turn it off and the base of $Q_2$ is forward biased to turn it on. Transistor $Q_2$ begins to turn on and reaches conduction at time $t_{on, Q_2}$. Because of its storage time delay, transistor $Q_1$ remains saturated and conducting; it does not turn off until time $t_{off, Q_1}$. Since $t_{off, Q_1}$ is greater than $t_{on, Q_2}$, both transistors are on for an interval of time shown as $\Delta t$ in figure 3. This period of time is the switching interval when shoot-through currents exist in the circuit. The value for $\Delta t$ is $t_{off, Q_1} - t_{on, Q_2}$ or, more generally,

$$\Delta t = t_{off} - t_{on} \tag{1}$$

when all of the transistors in the bridge circuit have the same $t_{on}$ and $t_{off}$ switching times.

Although the explanation to this point has been concerned with only one leg of the bridge, the same switching interval, $\Delta t$, exists at the same time in the other leg because the diagonal transistor pairs are switched together. The total result is that the battery or power source is short circuited by both legs of the bridge circuit and the load is also short circuited. The short-circuit conditions recur every half-cycle of the driving frequency.

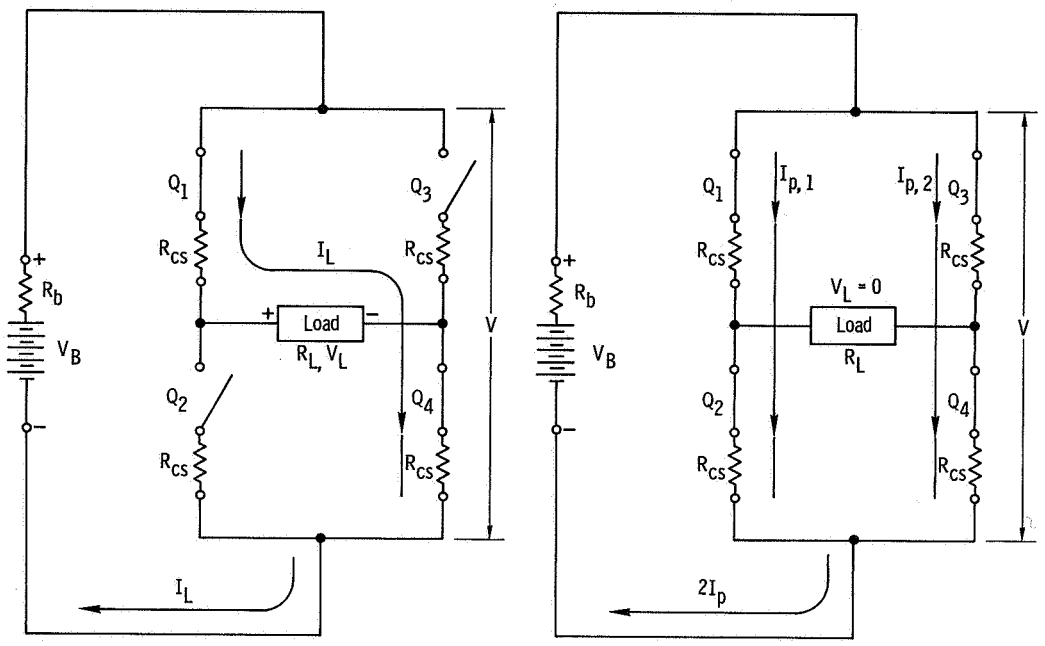
## SHOOT-THROUGH CURRENT

### Bridge Circuit With Single Transistors

For analytical purposes a switching transistor is often represented by a single-pole, single-throw switch. The closed position represents the transistor in the on, conducting, state and the open position represents the off, nonconducting state. With this substitution the equivalent circuits for the bridge circuit in figure 1 just prior to the switching time $t_o$, and during switching interval $\Delta t$, are as shown in figure 4.

Prior to the switching time $t_o$, during the positive half-cycle of the output load voltage, the load current $I_L$, shown in figure 4(a), flows through the conducting transistors $Q_1$ and $Q_4$. The magnitude of the load current is

$$I_L = \frac{V_B}{R_b + R_L + 2R_{cs}} \tag{2}$$




(a) Equivalent bridge circuit just prior to switching interval Δt. (b) Equivalent bridge circuit during switching interval Δt.

Figure 4. - Equivalent bridge circuit just prior to and during switching interval Δt.

No current flows through transistors $Q_2$ and $Q_3$ since these transistors are in the off state at this time.

During the switching interval, all of the transistors in the bridge are in the on, saturated conduction state, and it is assumed the transistors remain saturated for the entire interval Δt. The circuit in figure 4(b) represents this condition. The load voltage goes to zero during the interval Δt, and the magnitude of the shoot-through current through each transistor is

$$I_{p1} = I_{p2} = \frac{V_B}{2(R_b + R_{cs})} \tag{3}$$

The shoot-through currents then for a given source voltage are limited only by the internal resistance of the source and the saturated resistance of the transistors. They can reach damagingly high peak values, particularly when low impedance voltage sources are used to power the circuit. In practical circuits, using battery sources, the peak value of the shoot-through current can exceed the maximum-current rating of the transistor by an order of magnitude or more.

## Bridge Circuit with Paralleled Transistors

The equivalent circuit during the switching interval $\Delta t$ for the bridge circuit of figure 1 with parallel connected transistors is shown in figure 5(a). The circuit in this case contains four transistor banks, A to D, and each bank contains four transistors, $Q_1$ to $Q_4$. $I_{p,t}$ is the total shoot-through current through each bank and $I_{p,1}$, $I_{p,2}$, $I_{p,3}$, and $I_{p,4}$ are the individual shoot-through currents through each transistor in a bank. The conditions assumed for this circuit are as follows:

(1) The saturation resistance $R_{cs}$ for all transistors are equal.

(2) The turnon time for each transistor is less than the turnoff time of the fastest switching transistor in the circuit. This condition implies that the transistors in banks B and C are all on before the transistors in banks A and D turn off.

The shoot-through currents will be determined for equal and unequal turnoff characteristics.

Case 1: Equal turnoff time. - The condition for which all of the transistors have the same turnoff time is an ideal case and may be approached in practice by carefully screening and matching transistor switching characteristics. For this condition, the transistors are all turning off together and the analysis is the same as for single transistors. From equation (3) the general equation for the total shoot-through current through each transistor bank is

$$I_{p,t} = \frac{V_B}{2\left(R_b + \frac{R_{cs}}{n}\right)} \tag{4}$$

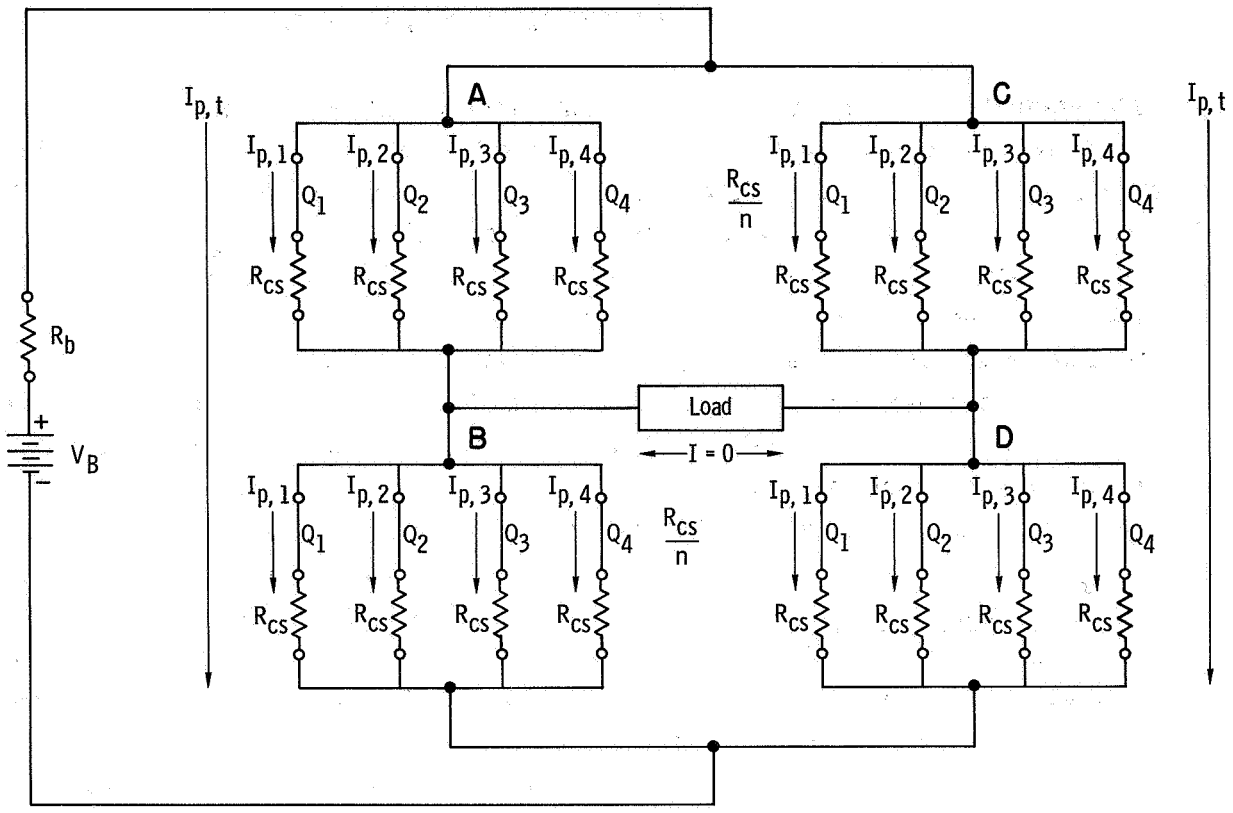
where n is the number of transistors paralleled in a bank.

Since equal saturation resistance implies equal division of $I_{p,t}$ among the paralleled transistors, the general equation for the shoot-through current through each transistor is

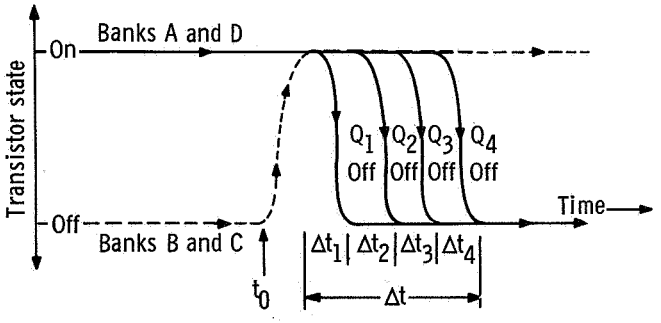
$$I_{p,1} = I_{p,2} = I_{p,3} = I_{p,4} = \cdots = I_{p,n} = \frac{V_B}{2n\left(R_b + \frac{R_{cs}}{n}\right)} \tag{5}$$

The expression for the individual shoot-through currents as a function of the total current is

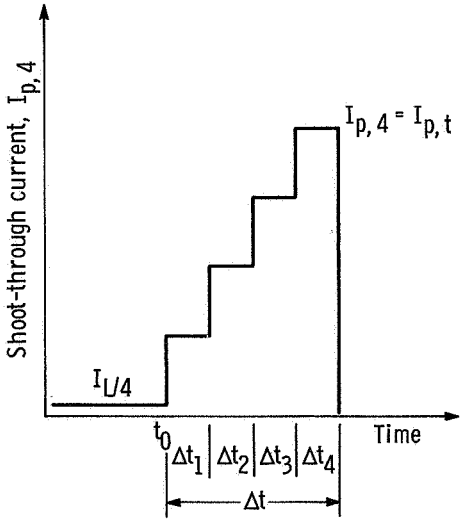
$$I_{p,1} = I_{p,2} = I_{p,3} = I_{p,4} = \cdots = I_{p,n} = \frac{I_{p,t}}{n} \tag{6}$$




(a) Equivalent circuit during switching interval Δt with parallel connected transistors.




(b) Assumed turnoff sequence of four parallel connected transistors.




(c) Shoot-through current through $Q_4$, slowest switching transistor in paralleled bank.

Figure 5. - Bridge circuit with parallel connected transistors.

This expression indicates that the magnitude of the shoot-through current through each transistor can be reduced by paralleling. This reduction is regarded as an advantage for parallel connected transistors.

In practical circuits $R_b > R_{cs}$ and $R_{cs}/n$ becomes a negligible quantity as n increases. For large values of n, equation (4) reduces to a constant current which is determined by the voltage and internal resistance of the source

$$I_{p,t} \cong \frac{V_B}{2R_b} \tag{7}$$

Case 2: Unequal turnoff time. - The condition for which each transistor in the bank has a different turnoff time is the typical condition generally encountered with paralleled transistors. The analysis becomes more burdensome for this case because the total switching interval $\Delta t$ must be subdivided into subintervals and the currents determined for each subinterval. For this case, the turnoff times of the paralleled transistors for each bank in figure 4(a) are assumed as shown in figure 5(b). Following the switching time $t_o$, the transistors in banks B and C are turned on before the transistors in banks A and D turn off. The transistors turn off in sequence; $Q_1$ is the first transistor to turn off and $Q_4$ is the last. The total switching interval is subdivided into four subintervals, $\Delta t_1$, $\Delta t_2$, $\Delta t_3$, and $\Delta t_4$ as shown.

The same general equations (eqs. (4) and (5)) are used to determine the total shoot-through current and the individual current through each of the transistors. It is necessary, however, to consider each subinterval of $\Delta t$ because the parallel resistance value of $R_{cs}$ for the banks turning off changes as each transistor turns off. The total shoot-through current through each leg of the bridge is

$$I_{p,t} = \frac{V_B}{2R_b + \frac{R_{cs}}{n} + \frac{R_{cs}}{m}} \tag{8}$$

where m is the number of transistors which are still conducting. The shoot-through current through each transistor in banks B and C is

$$I_{p,1} = I_{p,2} = I_{p,3} = I_{p,4} = \frac{I_{p,t}}{n} = \frac{V_B}{n\left(2R_b + \frac{R_{cs}}{n} + \frac{R_{cs}}{m}\right)} \tag{9}$$

where m = 4, 3, 2, and 1 for $\Delta t_1$, $\Delta t_2$, $\Delta t_3$, and $\Delta t_4$, respectively, and n = 4.

The shoot-through current for each transistor in banks A and D is as follows:

(1) During $\Delta t_1$, all four of the transistors are conducting. From equation (9) $I_{p,1} = I_{p,2} = I_{p,3} = I_{p,4} = I_{p,t,1}/4$ where n = 4, m = 4, and $I_{p,t,1}$ is the total shoot-through current during $\Delta t_1$.

(2) During $\Delta t_2$, $I_{p,1} = 0$ and $I_{p,2} = I_{p,3} = I_{p,4} = I_{p,t,2}/3$ where n = 3, m = 3, and $I_{p,t,2}$ is the total shoot-through current during $\Delta t_2$.

(3) During $\Delta t_3$, $I_{p,1} = I_{p,2} = 0$ and $I_{p,3} = I_{p,4} = I_{p,t,3}/2$ where n = 2, m = 2, and $I_{p,t,3}$ is the total shoot-through current during $\Delta t_3$.

(4) During $\Delta t_4$, $I_{p,1} = I_{p,2} = I_{p,3} = 0$ and $I_{p,4} = I_{p,t,4}$ where n = 1, m = 1, and $I_{p,t,4}$ is the total shoot-through current during $\Delta t_4$.

A sketch of the buildup of shoot-through current through transistor $Q_4$ in banks A and D for the entire interval $\Delta t$ is shown in figure 5(c). The assumptions for this figure are that $I_{p,t}$ is several times the maximum-current rating for the transistor and the normal load current design point is considerably less than the maximum-current rating. Figure 5(c) illustrates that the current surges through the slowest switching transistor in a group of paralleled transistors increases as each of the faster transistors turn off and will carry the total shoot-through current surge before it turns off.

## Effects of Shoot-Through Current

The predictability of transistor failures resulting from shoot-through current surges involves a degree of uncertainty because the exact limits of safe operating conditions for power transistors are not known precisely. Random failures have occurred for transistors supposedly operating within maximum ratings and established safe limits. The limits and ratings are based not only on the thermal capacity and characteristics of the transistor as a whole, but also on the thermal characteristics and conditions of the immediate surroundings. On these bases then, a transistor is likely to fail catastrophically when the power of a given shoot-through current spike or several recurring spikes causes the heat capacity and maximum junction temperature of the transistor to be exceeded. Failures of this type are predictable from a consideration of overall circuit operation and conditions. The area of uncertainty stems from the transistors which fail when subjected to shoot-through current spikes of low power content but relatively high current peaks. Investigations of such failures show that secondary breakdown is the immediate cause of failure. Secondary breakdown is a condition wherein the output impedance of a junction transistor changes abruptly from a large positive value to a negative value and then finally to a small positive value (ref. 2). The degradation within the transistor produced by current spikes is cumulative and leads to this failure mode. The current spike produces a

localized hot-spot within the transistor. The temperature is not high enough initially to cause extensive melting within the junction but only localized melting. The molten area however distorts the transistor's characteristics and this leads to failure by secondary breakdown. Transistor failures by secondary breakdown have been reported for a converter with parallel connected power transistors. The failures were confirmed to have occurred during the turnoff switching time interval of the power transistors (ref. 1).

Similar failures were experienced with an experimental pulse-width-modulated inverter using bridge circuits in the power stage and operating at a carrier frequency of approximately 10 kilohertz (refs. 10 and 3 (pp. 15, 18, and 26)). In the second case, however, the transistor failures were attributed to shoot-through currents. No analysis was made to determine a more specific identification with secondary breakdown or other failure mode. An effort was directed toward finding a solution to eliminate the failures. This effort results in the use of a reactor to protect the transistor from the current surges during the switching interval. The reactor technique was successful in eliminating transistor failures due to shoot-through currents.

## THE PROTECTIVE REACTOR

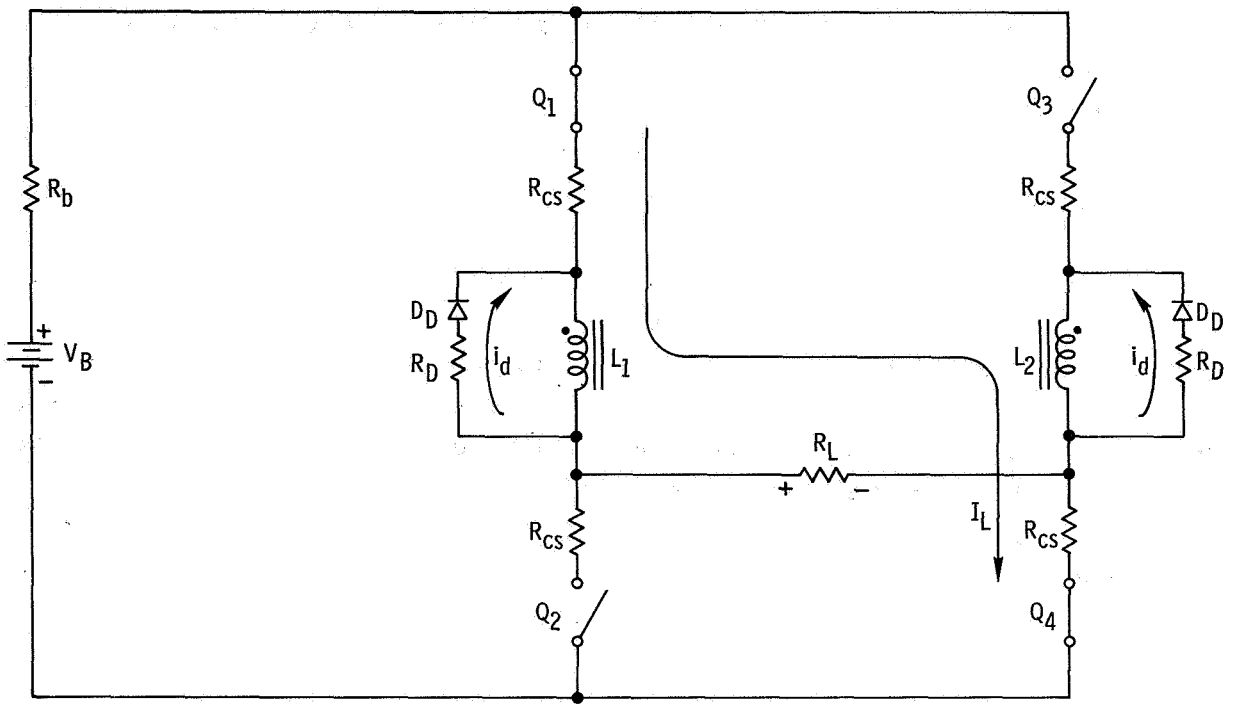
### Inductance Determination

The equivalent circuit of the transistor bridge circuit of figure 1 with protective reactors is shown in figure 6(a). Reactors $L_1$ and $L_2$ are in series with the transistors they protect and limit the current through the transistors during the switching interval $\Delta t$. The energy stored in each reactor by the shoot-through current is discharged through diode $D_D$ and resistor $R_D$. The discharge current $i_d$ flows through $D_D$ and $R_D$ after the completion of the switching interval.

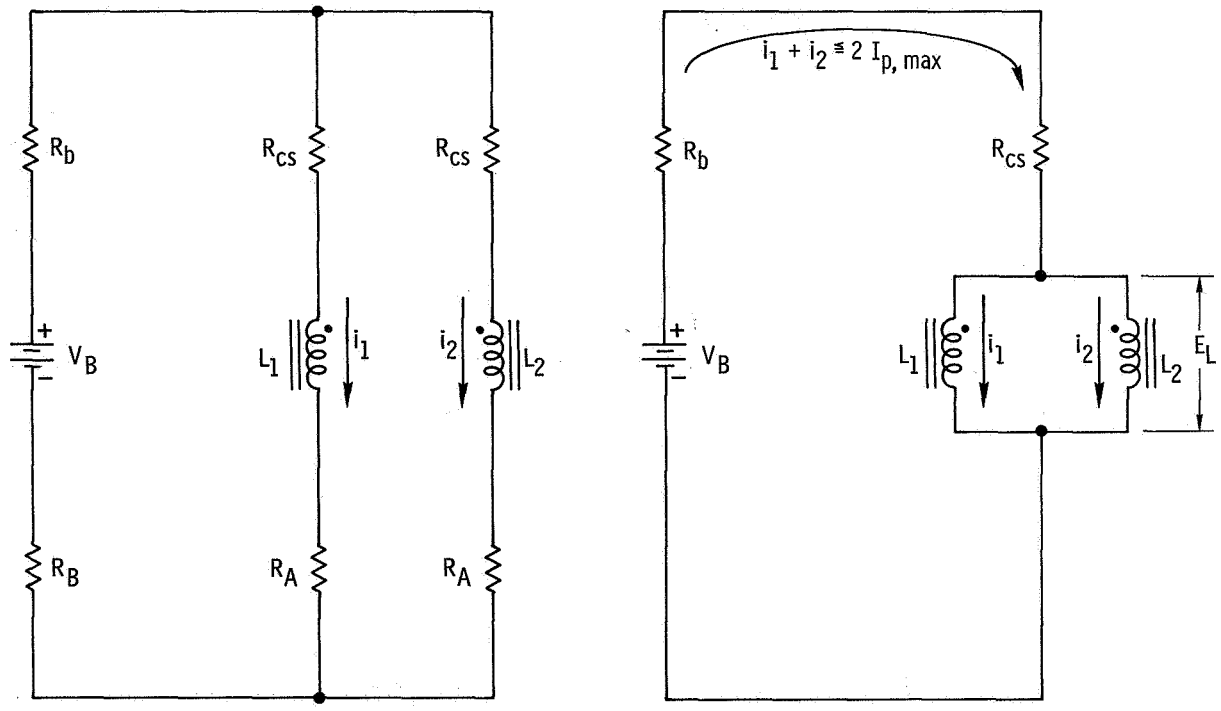
The value of inductance required to limit the shoot-through currents to a safe level ($I_{p,\,max}$) can be determined from an analysis of the equivalent circuit during the switching interval. This analysis is presented in appendix A for the equivalent circuit shown in figure 6(b). The shoot-through currents are $i_1$ and $i_2$. The initial conditions for $i_1$ and $i_2$ at the start of the switching interval are $i_1 = I_L$, the load current, and $i_2 = 0$.

By this analysis

$$i_1 = \frac{I_L}{2}\left(e^{-t/\tau_1} + e^{-t/\tau_2}\right) + \frac{V_B}{2(R_b + R_{cs})}\left(1 - e^{-t/\tau_2}\right) \tag{10}$$




(a) Equivalent transistor bridge circuit with protective reactors.




(b) Equivalent transistor bridge circuit with protective reactors during switching interval $\Delta t$.
$R_A = R_L R_{cs}/(R_L + 2\,R_{cs})$; $R_B = R_{cs}^2/(R_L + 2\,R_{cs})$.

(c) Simplified equivalent circuit assuming reactor voltage $E_L$ constant during switching interval $\Delta t$. $R_L \gg R_{cs}$.

Figure 6. - Equivalent circuits of transistor bridge with protective reactors before and during switching interval $\Delta t$.

$$i_2 = \frac{I_L}{2}\left(e^{-t/\tau_2} - e^{-t/\tau_1}\right) + \frac{V_B}{2(R_b + R_{cs})}\left(1 - e^{-t/\tau_2}\right) \tag{11}$$

where

$$\tau_1 = \frac{L(R_L + 2R_{cs})}{2R_{cs}(R_L + R_{cs})} \tag{12}$$

and

$$\tau_2 = \frac{L}{2(R_b + R_{cs})} \tag{13}$$

These equations do not explicitly express the currents as a function of the inductance but rather the inductance is contained in the time constants $\tau_1$ and $\tau_2$. Further solution to determine the value of $L$ required to limit $i_1$ and $i_2$ to some safe level $I_{p,\,max}$ during the switching interval $\Delta t$ requires that the circuit constants (i.e., $V_B$, $R_b$, and $R_{cs}$) be known. With the constants known, equations (10) and (11) can be solved graphically or by an iterative numerical method to determine the required inductance $L$ of the reactors.

## Approximate Method

In practical circuits the load resistance $R_L$, which is much larger than the saturated resistance of the transistors $R_{cs}$, which shunts $R_L$, can generally be neglected. The values for $R_{cs}$ and $R_b$ are approximately 0.10 ohm or less and the inductance of the reactors is very small, generally less than 100 microhenries. The time constants $\tau_1$ and $\tau_2$ of equations (10) and (11), evaluated with the aforementioned constants then are very long with respect to $\Delta t$. With the ratios of $\tau_1/\Delta t$ and $\tau_2/\Delta t$ large, the current rise through the reactors during $\Delta t$ is essentially linear which implies that a constant voltage exists across the reactors during this time. With this assumption of constant voltage, the equivalent circuit reduces to the circuit shown in figure 6(c).

The average voltage across the reactors $L_1$ and $L_2$ is

$$E_L = V_B - I_{p,\,max}(R_b + R_{cs}) = L_1\frac{di_1}{dt} = L_2\frac{di_2}{dt} \tag{14}$$

and

$$E_L \int_0^{\Delta t} dt = L_1 \int_{I_L}^{I_{p,\max}} di_1 = L_2 \int_0^{I_{p,\max}} di_2 \tag{15}$$

From equation (15)

$$L_1 = \frac{E_L \Delta t}{I_{p,\max} - I_L} = \frac{[V_B - I_{p,\max}(R_b + R_{cs})]\Delta t}{I_{p,\max} - I_L} \tag{16}$$

and

$$L_2 = \frac{E_L \Delta t}{I_{p,\max}} = \frac{[V_B - I_{p,\max}(R_b + R_{cs})]\Delta t}{I_{p,\max}} \tag{17}$$

Because the limits for $i_1$ and $i_2$ interchange on alternate switching intervals, the inductance for each reactor is determined from equation (16) which gives a larger value of inductance.

The inductance value of reactors for a practical circuit is determined in appendix B by the aforementioned approximate method and by the more exact equation (10). The error resulting from the use of the approximation is 15 percent for this example. This error is in a direction which results in a larger inductance and consequently more protection for the transistors so that the error is not detrimental to the circuit.

## Core Dimensions

The equation expressing the instantaneous voltage of a reactor in terms of the current, number of turns, inductance, and magnetic flux in the core of the reactor is

$$e_L = L\frac{di}{dt} = N\frac{d\varphi}{dt}\times 10^{-8}, \qquad V \tag{18}$$

and

$$\int e_L\, dt = L \int di = N \int d\varphi \times 10^{-8} \tag{19}$$

where $\varphi$ is the magnetic flux in maxwells or lines (where 1 Wb = $10^{-8}$ Mx).

With the assumptions used in the approximate method for determining inductance, equation (19) becomes

$$E_L \Delta t = L(I_{p,\,max} - I_L) = L\,\Delta I = N\,\Delta\varphi \times 10^{-8} \tag{20}$$

The relationship between the flux and area of a core is

$$\varphi = BA_c \tag{21}$$

and

$$\Delta\varphi = A_c\,\Delta B \tag{22}$$

where $A_c$ is the area of the core and $B$ is the flux density of the core material. By substitution of equation (22) into equation (20), the area of the core can be determined on the basis of the volt-seconds absorbed by the reactor during the switching interval and the change in the operating flux density of the core, that is,

$$A_c = \frac{E_L\,\Delta t \times 10^8}{N\,\Delta B} \tag{23}$$

From equation (14)

$$A_c = \frac{[V_B - I_{p,\,max}(R_b + R_{cs})]\Delta t \times 10^8}{N\,\Delta B} \tag{24}$$

The core area can be made small by operating the core over as large a $\Delta B$ range as possible without saturating the core. A typical magnetization curve of flux density $B$ plotted against magnetizing force $H$ is illustrated in figure 7 for a cut C-core of 3 percent silicon-iron magnetic material. The operating flux density range $\Delta B$ for a core with this material should not extend beyond a flux density of approximately 13.5 kilogauss (1.35 T) in order to avoid saturating the core.

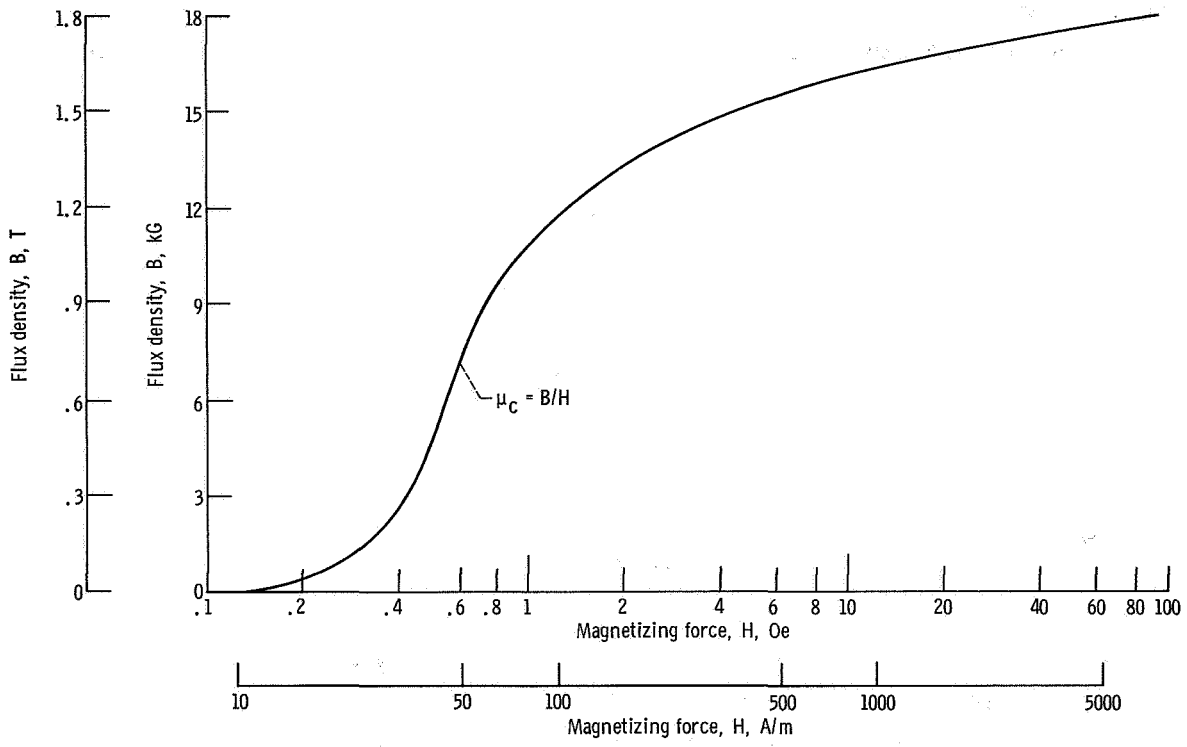



Figure 7. - Magnetization curve of 2-mil, 3 percent silicon-iron material for cut C-cores. Space factor, 89 percent.

From equations (20) and (22), the inductance of the core in terms of the core area and flux density is

$$L = \frac{N \Delta\varphi \times 10^{-8}}{\Delta I} = NA_c \frac{\Delta B}{\Delta I} \times 10^{-8} \tag{25}$$

The magnetizing force of a core is

$$H = 0.4\pi \frac{NI}{l} \tag{26}$$

and

$$\Delta H = \frac{0.4\pi N \Delta I}{l_c} \tag{27}$$

where H is the magnetizing force, NI is the magnetomotive force (mmf) in ampere turns, and $l_c$ is the length of the core.

From equations (25) and (27), the following equation is derived:

$$L = \frac{0.4\,\pi N^2 A_c}{l_c} \frac{\Delta B}{\Delta H} \times 10^{-8} \tag{28}$$

The ratio $\Delta B/\Delta H$ is the permeability $\mu$ of a magnetic material so that with this substitution, the inductance of a reactor is

$$L = 0.4\,\pi N^2 \frac{A_c}{l_c} \mu \times 10^{-8} \tag{29}$$

## Core with Air Gap

The permeability of most magnetic materials is generally so high that it is not practical to obtain the low values of inductance required for protective reactors by reducing the core area, the number of turns, or by increasing the core length. The usual practice is to determine the core area and turns in accordance with equation (24) for a low-core loss, high permeability magnetic material with high saturation flux density and then adjust the total inductance of the reactor by the inclusion of an air gap of the proper length in the magnetic circuit.

The air gap is in series with the core and a series magnetic circuit is analogous to an electric circuit with series-connected resistors. The analogous quantities are magnetic flux $\varphi$ and current I, magnetomotive force in ampere turns NI and voltage E, and magnetic reluctance $\mathscr{R}$ and electrical resistance R.

The reluctance of a magnetic circuit element is

$$\mathscr{R} = \frac{l}{\mu A} \tag{30}$$

and the equation for a series magnetic circuit with a magnetic flux $\varphi$ established in the circuit is

$$0.4\,\pi NI = \varphi (\mathscr{R}_{\text{core}} + \mathscr{R}_{\text{air gap}}) \tag{31}$$

and

$$0.4\,\pi N\,\Delta I = \Delta\varphi\left(\frac{l_c}{\mu_c A_c} + \frac{l_g}{\mu_g A_g}\right) \tag{32}$$

where the subscript c refers to the core and g refers to the air gap.

The permeability of air and vacuum $\mu_g$ is unity and, if fringing and leakage flux around the air gap are neglected, the area of the gap and core are equal in a series circuit, that is, $A_g = A_c$. From equation (32) then

$$\Delta\varphi = \frac{0.4\,\pi N\,\Delta I\,A_c}{\left(\frac{l_c}{\mu_c} + l_g\right)} \tag{33}$$

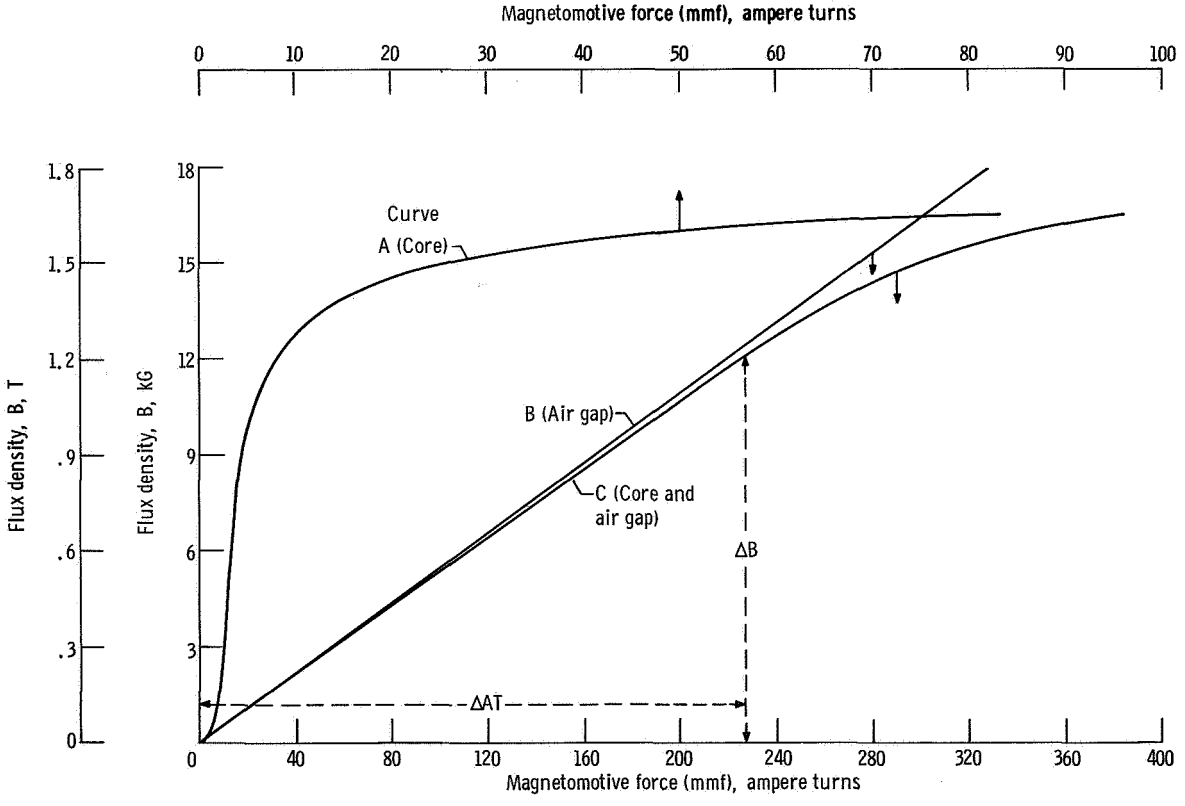



Figure 8. - Flux density plotted against magnetomotive force for C-core with air gaps.

Substituting $\Delta\varphi$ (eq. (33)) into equation (25) gives

$$L = \frac{0.4\,\pi N^2 A_c \times 10^{-8}}{\left(\frac{l_c}{\mu_c} + l_g\right)} \tag{34}$$

The effect of the air gap is to reduce the inductance of the reactor by requiring more ampere turns for a given flux density operating range $\Delta B$. This is illustrated by the curves in figure 8 for a C-core with air gaps. The $\Delta AT$ required for the $\Delta B$ operating range of the core and air gap combined (curve C) is much greater than the $\Delta AT$ required for the same $\Delta B$ in the core alone (curve A).

## Power Losses

Reactor loss. - The currents through the protective reactors are unidirectional so that the cores operate in the first quadrant of the characteristic $\varphi$ against AT operating loop. Because of this, it is necessary to reset the flux in the core at the completion of a switching interval to avoid saturating the core during the next and subsequent switching intervals. It is during reset that the energy stored in the reactors is dissipated as a power loss.

The first quadrant of a typical flux against ampere turn operating loop for a conventional magnetic material is illustrated in figure 9. This is a major loop and it is assumed that the flux excursions for the protective reactors traverses a minor loop, ABCDA, within the confines of the major loop. The flux excursions for the individual reactors can be explained in conjunction with figures 6(a) and (b). Prior to the start of the switching interval transistors, $Q_1$ and $Q_4$ are on and the load current $I_L$ flows through through reactor $L_1$. Transistors $Q_2$ and $Q_4$ are off at this time so that the current through reactor $L_2$ is zero. The magnetomotive force applied to $L_1$ is $NI_L$ and the flux in the core is $\varphi_L$. The flux in reactor $L_2$ is the remanent flux $\varphi_r$. During the switching interval, all of the transistors are conducting as shown in figure 6(b) and the currents through reactors $L_1$ and $L_2$ increase toward $I_{p,\,max}$. The magnetomotive force applied to each reactor is $NI_{p,\,max}$ and the flux in both reactors increases toward $\varphi_c$.

At the completion of the switching interval $\Delta t$, transistors $Q_1$ and $Q_4$ turn off, and transistors $Q_2$ and $Q_3$ remain on to conduct the load current $I_L$ through the load $R_L$ in the opposite direction. The current through reactor $L_2$ decreases to $I_L$ and the flux decreases to $\varphi_L$ (shown by the dashed line from points E to B in fig. 9).

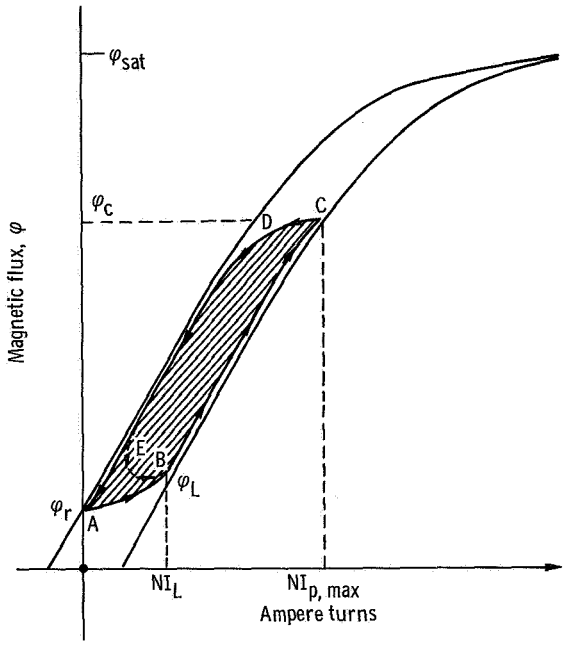



Figure 9. - Operating magnetic flux plotted against magnetomotive force loop for reactor core.

Both $R_D$ and $D_D$ (fig. 6(a)) provide a path for current $i_d$ to flow-through reactor $L_1$ to discharge the stored energy and reset the flux in the core. The resistance of $R_D$ is selected so that the time constant $L_1/R_D$ will permit the core to completely discharge within the half-cycle of the operating frequency and before the start of the next switching interval. The flux in reactor $L_1$ decreases to $\varphi_r$ while $i_d$ decays to zero. The energy stored in reactor $L_1$ is completely dissipated in $R_D$ by the reset current $i_d$.

Loss for circuit with reactors. - The power loss in the circuit (fig. 6(b)) during the switching interval results from discharging the energy stored in the reactors by the shoot-through currents. This power loss is essentially the power delivered by the source during $\Delta t$ and can be determined from

$$P_{avg} = 2f \int_0^{\Delta t} V_B(i_1 + i_2)\, dt \tag{35}$$

where

$$i_1 + i_2 = \left[2\left(\frac{I_{p, max} - I_L}{\Delta t}\right)t + I_L\right] \tag{36}$$

during the interval $\Delta t$.

By substituting equation (36) into equation (35) and performing the integration, the power loss is shown to be

$$P_{avg} = 2fV_B I_{p,\,max}\,\Delta t, \qquad W \tag{37}$$

Loss for circuit without reactors. - The shoot-through currents for the circuit in figure 4(b) were shown by equation (3) to be

$$I_{p1} = I_{p2} = \frac{V_B}{2(R_b + R_{cs})}$$

The total average power loss due to these shoot-through currents is

$$P_{avg} = 2f\,\Delta t\,\frac{V_B^2}{(R_b + R_{cs})}, \qquad W \tag{38}$$

This power loss (provided the transistors survive the high current peaks) is very much greater than the power loss with the reactors as shown by equation (37). Calculations of power losses for the circuit considered in appendix B shows the power loss of the circuit with reactors is only 5 percent of the power loss of the circuit without the reactors.

## Split Reactor Configurations

The split reactor is sometimes used in circuit applications where a single reactor is physically too large to be practical and in parallel transistor configurations for which the transistors do not equally share the total load current. The circuit in figure 10 illustrates the split reactor for a bridge circuit with single connected transistors. Each reactor is designed for an inductance equal to one-half the inductance of a single reactor for the same application. A separate diode and discharge resistor is used for each reactor as shown.

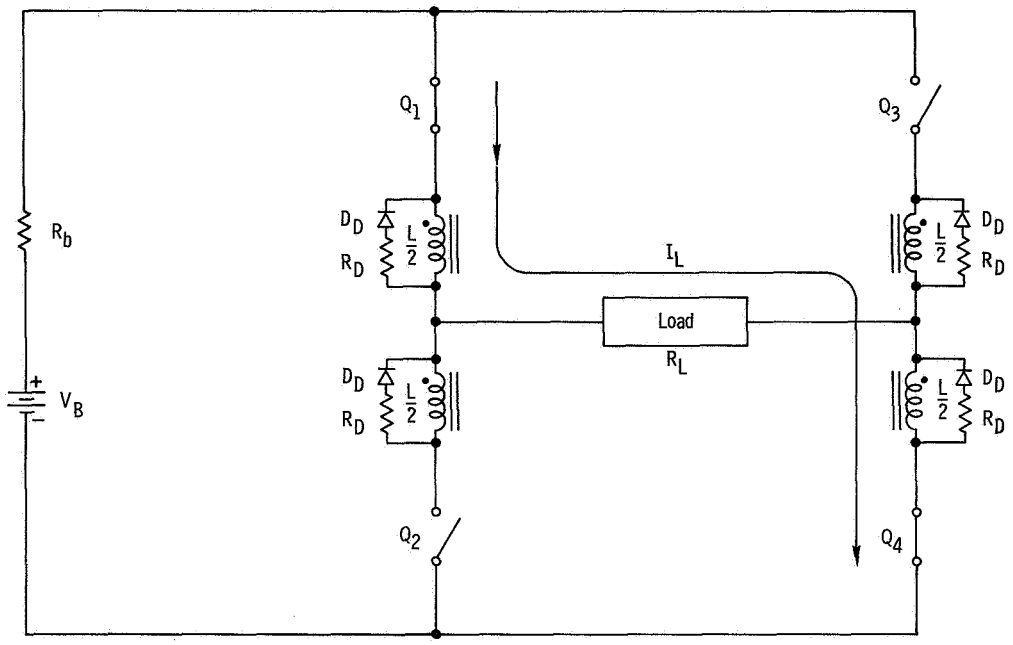



Figure 10. - Bridge circuit with split reactors.

## Reactors for Paralleled Transistors

The use of a single large reactor for protection of parallel connected transistors (similar to the configuration in fig. 6(a)), presents the possibility of progressive failures (chain-reaction) from an initial failure of a single transistor whose switching characteristics have changed. The change in switching characteristics may be due to aging or some other reason. Because of this possibility, the single reactor configuration is not recommended for maximum protection of paralleled transistors.

The reactor configuration illustrated in figure 11 provides individual transistor protection by individual reactors and is recommended for parallel connected transistor circuits. Because of the differences in turnoff times among the transistors in the circuit, however, the inductance of each reactor is determined in accordance with equation (16) for the full voltage $E_L$ during $\Delta t$. This is in contrast to the split reactor configuration where the inductance is one-half the inductance of a single reactor. The switching interval $\Delta t$ for use in equation (16) should be determined on the basis of the fastest turnon time and the slowest turnoff time of all the transistors in the circuit. These considerations (i. e., full $E_L$ and large $\Delta t$) will provide an additional safety factor by means of a larger inductance than required.

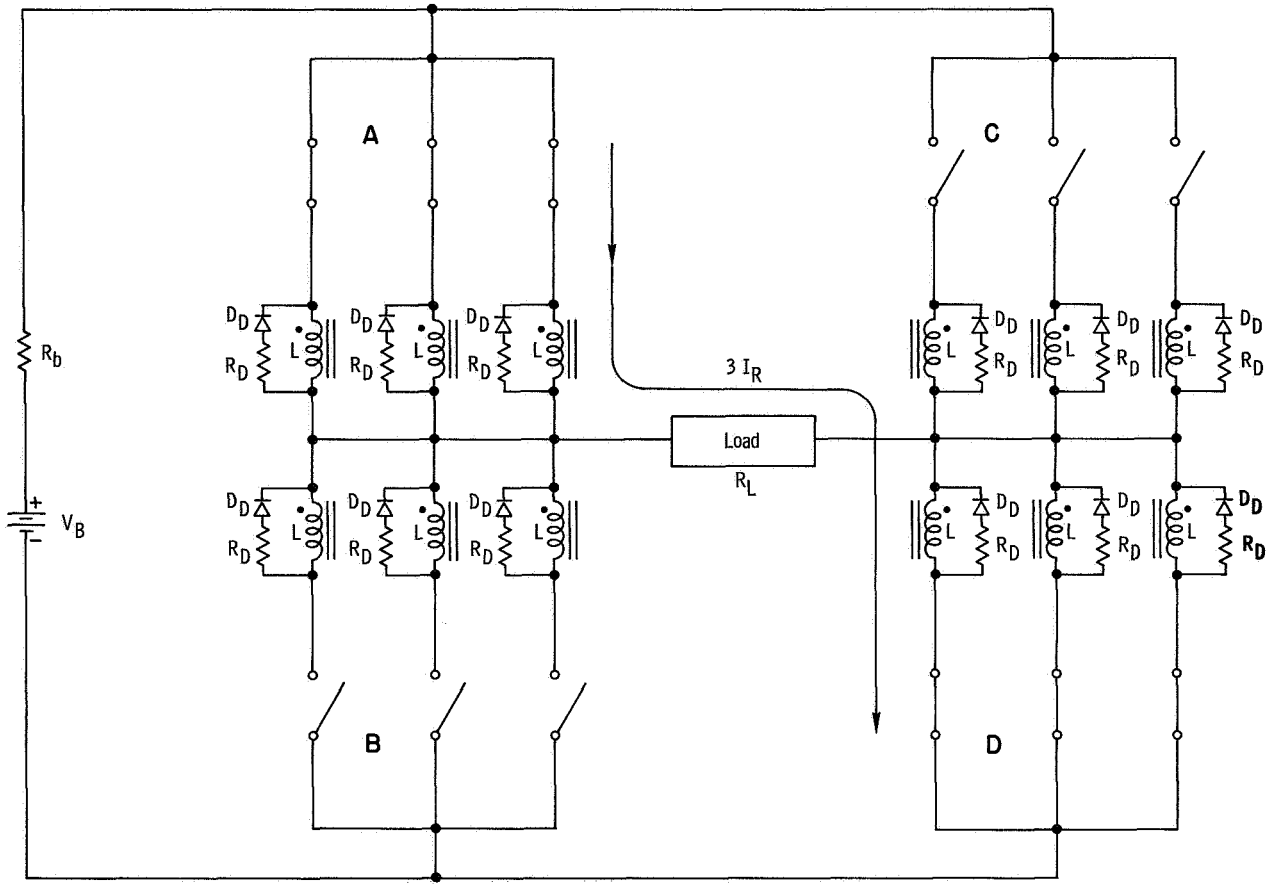



Figure 11. - Protective reactors for bridge circuit with paralleled transistors.

## DISCUSSION OF ANALYSIS

An underlying degree of conservatism is reflected in the analysis and reactor design primarily because of the unknown and uncertain factors and conditions concerning transistor failure modes. Since the experience with the experimental pulse-width-modulated bridge inverter circuit provided proof that transistors can fail as a result of shoot-through currents, the approach followed in the analysis and design was to be concerned not so much with how a transistor fails, but to avoid all operating conditions that could possibly lead to failure.

The particular assumption about which a question of validity may exist pertains to the transistors remaining saturated throughout the switching interval. This assumption is logical for circuits employing proportional feedback of collector current to the base drive circuit, but it is conceivable that one or both transistors in a given leg of a bridge

circuit with constant base drive could become unsaturated as the collector current rises rapidly. The transistors in this case then would be operating in the active linear region of the characteristic and failure could result from the secondary breakdown mechanism or from excessive power dissipation due to high collector-to-emitter voltage and current. The use of this assumption, however, coupled with the shoot-through current level criterion, results in a reactor design with a built-in safety factor. The conditions for which failures can occur are avoided, and the shoot-through current peaks are limited to levels within the recommended maximum peak value. In this way the transistors are operated at safe current levels and circuit reliability is enhanced.

The analysis and design are based on the success realized from the use of protective reactors in the experimental inverter. This inverter is a pulse-width-modulated inverter operating at a carrier frequency of 10 kilohertz and producing a sinusoidal, three-phase, 400-hertz output voltage of 120/208 volts. The input voltage is 56 volts dc. The inverter is rated at 5 kilowatts and utilizes a bridge circuit with parallel connected transistors in the output power stage. The protective reactors eliminated transistor failures due to shoot-through currents in this inverter circuit. The analysis and design method are sufficiently comprehensive to be useful in designing reactors for specific applications. The approximate method is sufficiently accurate to facilitate the design of reactors to practical fabrication tolerances. The application of the method and the design equations to a practical system is described and illustrated in appendix B of this report.

## CONCLUDING REMARKS

A theoretical analysis of the equivalent circuit of a transistor inverter bridge circuit shows that, because of the unequal switching characteristics of the transistors, the shoot-through currents that tend to flow through the transistors during the switching interval are limited only by the saturated resistance of the transistors and the internal resistance of the power source. The current peaks can reach levels an order of magnitude greater than the maximum-current rating of the transistors and can produce an exceptionally high power loss in the circuit even if the transistors survive.

The shoot-through currents can be limited to safe levels within the transistor's maximum-current rating by the use of protective reactors. The required inductance is determined on the basis of the maximum time difference between the turnon and turnoff switching characteristics of the transistors and the magnitude of the load voltage to be absorbed by the reactor during the switching interval. The approach of the reactor design technique presented is to protect the transistors by restricting the current surges to safe levels, avoiding those current levels and operating conditions that ultimately lead to transistor failure. This design technique produces a reactor of small size. The reac-

tors dissipate very little power and significantly reduce the power loss due to shoot-through currents; the power loss of a practical bridge circuit with reactors is only 5 percent of the power loss of the same circuit without the reactors.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, September 25, 1968,
120-27-03-28-22.

# APPENDIX A

## DERIVATION OF EQUATIONS FOR SHOOT-THROUGH CURRENTS

The transistor bridge circuit with protective reactors in each leg of the bridge is illustrated in figure 6(a). The transistors, $Q_1$ to $Q_4$, are represented by single-pole switches. The load current $I_L$ is shown flowing through transistors $Q_1$ and $Q_4$ and the load resistance $R_L$. Transistors $Q_2$ and $Q_3$ are off and nonconducting. This circuit condition is a steady-state condition during one-half cycle of the operating frequency. On the alternate half-cycle, transistors $Q_2$ and $Q_3$ are conducting, $Q_1$ and $Q_4$ are nonconducting, and the direction of the current $I_L$ through the load is reversed. During the switching interval $\Delta t$, all of the transistors are conducting and the circuit is in a transient state. The equivalent circuit for this period of time is shown in figure 6(b) in which the $\Delta$-network formed by $R_L$ and $R_{cs}$ of $Q_2$ and $Q_4$ in figure 6(a) has been replaced by the equivalent Y-network, $R_A$, $R_A$, and $R_B$.

The differential equations for the currents $i_1$ and $i_2$ in figure 6(b) are

$$V_B = (i_1 + i_2)(R_b + R_B) + i_1(R_A + R_{cs}) + L_1 \frac{di_1}{dt} \tag{A1}$$

$$V_B = (i_1 + i_2)(R_b + R_B) + i_2(R_A + R_{cs}) + L_2 \frac{di_2}{dt} \tag{A2}$$

By letting

$$R_c = R_A + R_{cs}$$

$$R_E = R_b + R_B$$

$$R_m = R_c + R_E$$

and

$$L_1 = L_2 = L$$

equations (A1) and (A2) are rewitten as

$$R_m i_1 + L\frac{di_1}{dt} + i_2 R_E = V_B \tag{A3}$$

$$R_m i_2 + L\frac{di_2}{dt} + i_1 R_E = V_B \tag{A4}$$

The Laplace transforms for equations (A3) and (A4) for the initial conditions of $i_1(0) = I_L$ and $i_2(0) = 0$ are

$$R_m \bar{i}_1 + sL\bar{i}_1 - LI_L + R_E \bar{i}_2 = \frac{V_B}{s} \tag{A5}$$

$$R_m \bar{i}_2 + sL\bar{i}_2 + R_E \bar{i}_1 = \frac{V_B}{s} \tag{A6}$$

and the solution yields

$$i_1(t) = \frac{I_L}{2}\left[e^{(R_E - R_m)t/L} + e^{-(R_E+R_m)t/L}\right] - \frac{V_B}{R_E + R_m}\left[e^{-(R_E+R_m)t/L} - 1\right] \tag{A7}$$

$$i_2(t) = \frac{I_L}{2}\left[e^{-(R_E+R_m)t/L} - e^{(R_E - R_m)t/L}\right] + \frac{V_B}{R_E + R_m}\left[1 - e^{-(R_E+R_m)t/L}\right] \tag{A8}$$

By reverting to the original resistance substitutions

$$i_1(t) = \frac{I_L}{2}\left\{e^{-[2R_{cs}(R_L+R_{cs})/L(R_L+2R_{cs})]t} + e^{-[2(R_b+R_{cs})/L]t}\right\}$$

$$+ \frac{V_B}{2(R_b + R_{cs})}\left\{1 - e^{-[2(R_b+R_{cs})/L]t}\right\} \tag{A9}$$

$$i_2(t) = \frac{I_L}{2}\left\{e^{-[2(R_b+R_{cs})/L]t} - e^{-[2R_{cs}(R_L+R_{cs})/L(R_L+2R_{cs})]t}\right\}$$

$$+\frac{V_B}{2(R_b + R_{cs})}\left\{1 - e^{-[2(R_b+R_{cs})/L]t}\right\} \qquad \text{(A10)}$$

By letting

$$\tau_1 = \frac{L(R_L + 2R_{cs})}{2R_{cs}(R_L + R_{cs})}$$

and

$$\tau_2 = \frac{L}{2(R_b + R_{cs})}$$

equations (A9) and (A10) simplify to

$$i_1(t) = \frac{I_L}{2}\left(e^{-t/\tau_1} + e^{-t/\tau_2}\right) + \frac{V_B}{2(R_b + R_{cs})}\left(1 - e^{-t/\tau_2}\right) \qquad \text{(A11)}$$

and

$$i_2(t) = \frac{I_L}{2}\left(e^{-t/\tau_2} - e^{-t/\tau_1}\right) + \frac{V_B}{2(R_b + R_{cs})}\left(1 - e^{-t/\tau_2}\right) \qquad \text{(A12)}$$

# APPENDIX B

## DESIGN OF PROTECTIVE REACTORS FOR A PRACTICAL BRIDGE CIRCUIT

The circuit without the protective reactors is the single-phase bridge circuit shown in figure 1. The circuit operates at a frequency of 400 hertz and produces a square wave output voltage to a resistive load of 5.86 ohms. The circuit is powered by a 60-volt, 100-ampere-hour, nickel-cadmium battery. The rated load current is 10 amperes. The silicon power transistors are type 2N2772.

The battery contains 45 cells for a 60-volt output. The resistance per cell is 0.0015 ohm, and the total internal resistance of the battery is $R_b = 0.0675$ ohm (ref. 6).

The characteristics of the transistor obtained from the published data sheet (ref. 7) are as follows:

$V_{CE} = 200$ V (max) $\qquad I_c = 30$ A dc (max)

$V_{CB} = 200$ V (max) $\qquad I_B = 7.5$ A dc (max)

$V_{EB} = 15$ V (max) $\qquad P_c = 200$ W at $T_{case} = 75^{\circ}$ C (max)

$$R_{CES} = \begin{cases} 0.037 \text{ ohm (typ)} \\ 0.075 \text{ ohm (max) at} \begin{cases} I_c = 20 \text{ A} \\ I_B = 4 \text{ A} \end{cases} \end{cases}$$

$$h_{FE} = \begin{cases} 10 \text{ min} \\ 12.5 \text{ min (typ) at} \begin{cases} V_{CE} = 4 \text{ V} \\ I_c = 20 \text{ A} \end{cases} \end{cases}$$

The range in switching characteristics for switching a collector current of 10 amperes with $I_b = \pm 3$ amperes is

$$\text{Turnon time} = \begin{cases} 2.8 \ \mu\text{s (min)} \\ 3.8 \ \mu\text{s (max)} \end{cases}$$

$$\text{Turnoff time} = \begin{cases} 9.0\ \mu s\ (\text{min}) \\ \\ 19.5\ \mu s\ (\text{max}) \end{cases}$$

## Switching Interval

From the aforementioned switching characteristics, the worst case switching interval is (eq. (1))

$$\Delta t = [t_{off}\ (\text{max}) - t_{on}\ (\text{min})] = (19.5 - 2.8) = 16.7\ \mu s$$

## Shoot-Through Currents

Circuit with single transistors. - The equivalent circuits for figure 1 just prior to and during the switching interval are shown in figure 4. The rated load current for this circuit is 10 amperes (i. e., $I_L = 10$ A). This is the current-through transistors $Q_1$ and $Q_4$ just prior to the switching interval.

The shoot-through current through each transistor during the switching interval is (eq. (3))

$$I_{p,1} = I_{p,2} = \frac{V_B}{2(R_b + R_{cs})} = \frac{60}{2(0.0675 + 0.037)} = 286\ \text{A}$$

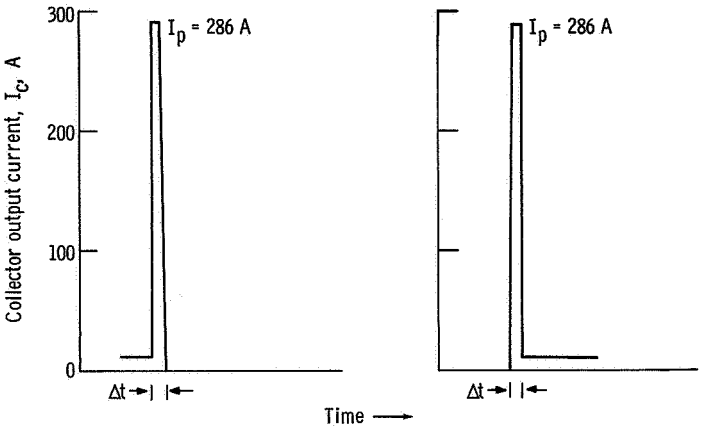
This current peak is nearly ten times the 30-ampere maximum-current rating for the transistor.

The current through the transistors just prior to, during, and immediately after the switching interval $\Delta t$ is illustrated in figure 12.

Circuit with paralleled transistors. - The equivalent circuit of the bridge circuit in figure 1 with four paralleled transistors per bank is shown in figure 5(a).

Case 1: Equal turnoff time: For this case, all of the transistors are assumed to have the same turnoff characteristic. The total shoot-through current through each bank of transistors is (eq. (4))

$$I_{p,t} = \frac{V_B}{2\left(R_b + \frac{R_{cs}}{n}\right)\Big|_{n=4}} = \frac{60}{2\left(0.0675 + \frac{0.037}{4}\right)} = 392\ \text{A}$$




(a) Current through transistors $Q_1$ and $Q_4$ just prior to and during switching interval Δt.

(b) Current through transistors $Q_2$ and $Q_3$ during switching interval Δt and immediately thereafter.

Figure 12. - Current through transistors just prior to, during, and immediately after switching interval Δt.

The shoot-through current through each transistor is (eq. (6))

$$I_{p,1} = I_{p,2} = I_{p,3} = I_{p,4} = \frac{I_{p,t}}{n} = \frac{392}{4} = 98 \text{ A}$$

Case 2: Unequal turnoff time: For this case, the turnoff characteristics for the transistors in the bank are unequal, and the characteristics for each bank are assumed as illustrated in figure 5(b). The switching interval is equal to

$$\Delta t = \Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 = 16.7 \ \mu s$$

and the subintervals are equal, that is,

$$\Delta t_1 = \Delta t_2 = \Delta t_3 = \Delta t_4 = \frac{16.7}{4} = 4.175 \ \mu s$$

The total shoot-through current through each transistor bank for each subinterval is (from eq. (8))

$$I_{p,t} = \frac{V_B}{2R_b + \frac{R_{cs}}{n} + \frac{R_{cs}}{m}} = \frac{60}{2 \times 0.0675 + \frac{0.037}{4} + \frac{0.037}{m}}$$

as follows:

(1) During $\Delta t_1$, m = 4 and $I_{p,t_1}$ = 60/0.1535 = 392 amperes.

(2) During $\Delta t_2$, m = 3 and $I_{p,t_2}$ = 60/0.1566 = 383 amperes.

(3) During $\Delta t_3$, m = 2 and $I_{p,t_3}$ = 60/0.1628 = 369 amperes.

(4) During $\Delta t_4$, m = 1 and $I_{p,t_4}$ = 60/0.1813 = 333 amperes.

The shoot-through currents through each transistor in banks A and D which are turning off during the switching interval are (from eq. (9)) the following:

(1) During $\Delta t_1$, $I_{p,1} = I_{p,2} = I_{p,3} = I_{p,t_1}/4\Big|_{\substack{n=4\\m=4}}$ = 392/4 = 98 amperes.

(2) During $\Delta t_2$, $I_{p,1} = 0$ and $I_{p,2} = I_{p,3} = I_{p,4} = I_{p,t_2}/3\Big|_{\substack{n=3\\m=3}}$ = 383/3 = 128 amperes.

(3) During $\Delta t_3$, $I_{p,1} = I_{p,2} = 0$ and $I_{p,3} = I_{p,4} = I_{p,t_3}/2\Big|_{\substack{n=2\\m=2}}$ = 369/2 = 185 amperes.

(4) During $\Delta t_4$, $I_{p,1} = I_{p,2} = I_{p,3} = 0$ and $I_{p,4} = I_{p,t_4}\Big|_{\substack{n=1\\m=1}}$ = 333 amperes.

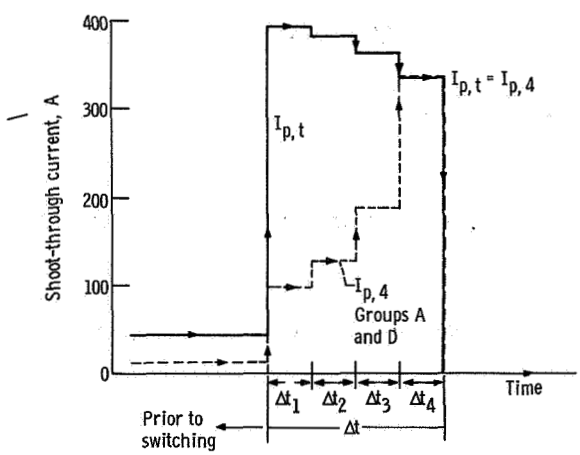



Figure 13. - Shoot-through currents for bridge circuit with four paralleled transistors.

The total shoot-through current through each transistor bank and the buildup of shoot-through current through $Q_4$, the slowest transistor in the group, is illustrated in figure 13.

## Protective Reactors For Single Transistors

Inductance calculation - approximate method. - The equivalent circuit for the bridge circuit in figure 1 with protective reactors is shown in figure 6(a). The rated load current $I_L$ is 10 amperes. The maximum current through each transistor $I_{p,\,max}$ is to be limited to the maximum-current rating of the transistor, and $I_{c,\,max}$ for the 2N2772 transistor is 30 amperes. The switching interval $\Delta t$ is 16.7 microseconds. The inductance of each reactor from the approximate method of equation (16) is

$$L = \frac{[V_B - I_{p,\,max}(R_b + R_{cs})]\Delta t}{I_{p,\,max} - I_L} = \frac{[60 - 30(0.0675 + 0.037)]16.7\times10^{-6}}{30 - 10} = 47.4\ \mu H$$

Exact method. - Equation (10) is an exact relationship between the current and inductance of the reactor. Equation (16) is an approximate relationship. Equation (10) for this particular circuit is

$$I_{p,\,max} = \frac{I_L}{2}\left(e^{-t/\tau_1} + e^{-t/\tau_2}\right) + \frac{V_B}{2(R_b + R_{cs})}\left(1 - e^{-t/\tau_2}\right)$$

$$= \frac{10}{2}\left(e^{-0.000033/L} + e^{-0.0000035/L}\right) + \frac{60}{2(0.0675 + 0.037)}\left(1 - e^{-0.0000035/L}\right)$$

A curve of $I_{p,\,max}$ as a function of $L$ is plotted in figure 14. From this curve, the inductance required to limit $I_{p,\,max}$ to 30 amperes is 41.25 microhenries. The error resulting from the use of the approximate relation (eq. (16)) is

$$\text{Error} = \frac{47.4 - 41.25}{41.25} \times 100 = 15 \text{ percent}$$

Discharge resistor $R_D$. The function of resistor $R_D$ (shown in fig. 5(a)) is to dissipate the energy in the reactor and reset the magnetic flux in the core during the half-cycle when its associated transistors are turned off. The time of a half-cycle of the

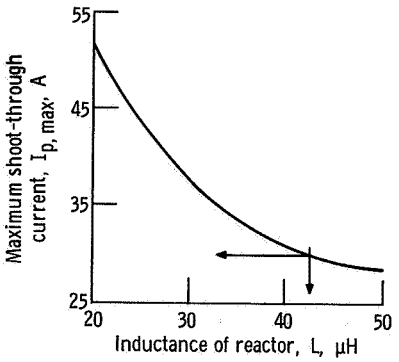



Figure 14. - Plot of maximum shoot-through current against inductance of reactor for exact solution of required inductance for protective reactors.

$I_{p, max} = \frac{I_L}{2}\left(e^{-0.000033/L} + e^{-0.0000035/L}\right)$

$\frac{V_B}{2(R_b + R_{cs})}\left(1 - e^{-0.0000035/L}\right)$. Required L = 41.25 microhenries to limit $I_{p, max}$ through transistors to 30 amperes.

400-hertz operating frequency is

$$t_p = \frac{1}{2}\left(\frac{1}{f}\right) = \frac{1}{2}\left(\frac{1}{400}\right) = 0.00125 \text{ s}$$

The time constant of the discharge circuit consisting of L and $R_D$ is $T_D = L/R_D$. Since the discharge current $i_d$ decreases exponentially, approximately six time constant periods are required to completely discharge the reactor. On this basis then, $t_D \leq t_p/6$ or $t_D \leq 0.000208$ second. The resistance value for $R_D$ then is

$$R_D = \frac{L}{0.000208} = \frac{47.4 \times 10^{-6}}{20.8 \times 10^{-5}} = 0.223 \text{ ohm}$$

In a practical circuit, it may be possible to obtain this required resistance in the forward resistance of the discharge diode and thereby eliminate $R_D$.

Power loss. - The average power loss of the circuit in figure 5(a) with protective reactors at the 400-hertz operating frequency is (from eq. (37))

$$P_{avg} = 2fV_B I_{p, max} \Delta t = 2 \times 400 \times 60 \times 30 \times 16.7 \times 10^{-6} = 24 \text{ W}$$

## Circuit Without Reactors

The average power loss of the circuit without the reactors (fig. 4(a)) is

$$P_{avg} = 2f(I_{p1} + I_{p2})V_B \Delta t$$

From equation (3)

$$I_{p,1} = I_{p,2} = \frac{V_B}{2(R_b + R_{cs})}$$

and

$$P_{avg} = 2f \frac{V_B^2}{(R_b + R_{cs})} \Delta t = \frac{2 \times 400 \times 60^2 \times 16.7 \times 10^{-6}}{0.0675 + 0.037} = 460 \text{ W}$$

The reduction in power loss resulting from the use of protective reactors is

$$\text{Reduction} = \frac{460 - 24}{460} \times 100 = 95 \text{ percent}$$

## Core Size

The selection of a core size involves some trial and error when available standard cores are to be used. A published magnetization curve for 2 mil, 3 percent silicon-iron core material commonly used in cut C-core configurations is shown in figure 7 (ref. 8, p. 32). The curve does not include the effects of the air gaps present in a C-core. The ace factor for determining the effective area of the core from this curve is 89 percent. The required area of the core determined from equation (24) is

$$A_c = \frac{[V_B - I_{p,max}(R_b + R_{cs})]\Delta t \times 10^8}{N \Delta B}$$

From figure 7, a change in flux density $\Delta B$ from 0 to 12 kilogauss (0 to 1.2 T) includes the linear region of the curve and is well below the saturated region. These operating points give a $\Delta B$ = 12 kilogauss (1.2 T). Substituting $\Delta B$ and the other known

parameters into equation (24) gives

$$A_c = \frac{[60 - 30(0.0675 + 0.037)]16.7\times10^2}{N \times 12\times10^3} = \frac{7.90}{N} \text{ cm}^2$$

Accounting for the space factor and converting to square inches, the gross area of the core is

$$A_c = \frac{7.90}{N} \frac{1}{6.45} \frac{1}{0.89} = \frac{1.375}{N} \text{ in.}^2$$

Some trial and error is necessary at this point to arrive at the number of turns on the core. A large number of turns will give a small core area but could require a large window area to accommodate the turns. At this point assume $N = 10$. The required core area for 10 turns is

$$A_c = \frac{1.375}{10} = 0.1375 \text{ in.}^2$$

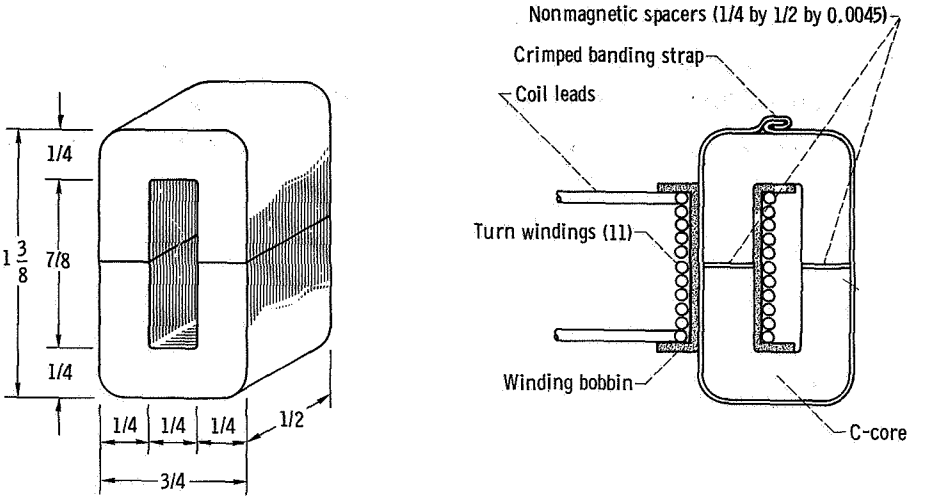
The standard cores with an area close to the required area with $N = 10$ have a gross area of 0.125 square inch. By making $N = 11$, $A_c = 1.375/11 = 0.125$ square inch, so that this core area is satisfactory. Two cores with window lengths of 7/8 and 1 inch are available with this core area (ref. 8, p. 34).

The selection of the core length will depend on the space required for the winding. The space for the winding is determined as follows. The rated load current through the reactor is 10 amperes. With an assumed current density of 400 circular mils per ampere, the required area of the wire is 4000 circular mils. Number 14, B&S gage wire has an area of 4100 circular mils and will be adequate. The diameter of the bare wire is 0.0641 inch and is assumed to be 0.07 inch for an insulated wire. The window length required for 11 turns is 0.77 inch so that the core with the 7/8-inch window length will accommodate the turns. A sketch of the core is shown in figure 15(a). The length of the mean magnetic path in the core is 2.93 inches or 7.45 centimeters.

The length of the air gap is determined from equation (34) as follows

$$l_g = \frac{0.4\,\pi N^2 A_c \times 10^{-8}}{L} - \frac{l_c}{\mu_c}$$

From figure 7, $\mu_c = 8880$ for $B = 12$ kilogauss (1.2 T). Substituting the values into the




(a) C-core for protective reactor; 2-mil, 3 percent silicon-iron core material. Gross core area, 0.125 square inch; mean length of magnetic path, 2.93 inches; space factor, 89 percent; weight, 0.091 pounds.

(b) Assembled reactor. Inductance, 47.4 microhenries.

Figure 15. - Core and assembled reactor. Scale: full scale. (All dimensions in inches.)

previous equation, the length of the air gap is

$$l_g = \frac{1.25 \times 11^2 \times 0.718 \times 10^{-8}}{47.4 \times 10^{-6}} - \frac{7.45}{8880} = 0.0229 \text{ cm} = 0.009 \text{ in.}$$

This length is the total length of the air gap. A C-core contains two air gaps in series, and the length of each gap is one-half of the total gap so that

$$\frac{l_g}{\text{each air gap}} = 0.0045 \text{ in.} = 0.01145 \text{ cm}$$

The air gap can be obtained by means of a nonmagnetic spacer. A sketch of the complete wound reactor is shown in figure 15(b). The magnetic characteristics of flux density B as a function of the applied ampere turns for this completed core are shown in figure 8. Curve A is the characteristic of the core without the air gaps. It is obtained from the curve shown in figure 7 for this specific core configuration by converting the H values to ampere turns; that is, $AT = 0.4\pi H l_c$. Curve B of figure 8 is a plot of flux density against ampere turns for the total air gap length of 0.0229 centimeter. Curve C is the operating characteristic curve for the completed core including the air gaps. This

curve is obtained by combining curves A and B. Because the flux density in the air gaps is the same as the flux density in the iron, curves A and B are combined by adding the ampere turns for a given flux density. The effect of the air gaps is to decrease the slope and extend the linear region of the curve. The protective reactor operates over the region indicated by $\Delta B$ and $\Delta AT$. The inductance will be constant because the region is linear and well below the saturation region of the core.

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